REMARKS

In the Office Action the Examiner objected to the drawings under 37 C.F.R. 1.83(a) for not showing every claimed feature, objected to the specification for not having a summary, rejected claims 1-34 under 35 U.S.C. 112, first paragraph, for failing to comply with the enablement requirement, rejected claims 1-2, 10, 14-15, 17, and 31-32 under 35 U.S.C. 112, second paragraph, for being indefinite, and rejected claims 1-34 under 35 U.S.C. 103 for being obvious. Claims 1-18, claims 20-26 and claims 28-34 remain in the application.

As for the lack of summary, applicants refer to 37 C.F.R. 1.73, which states, "Such summary, when set forth, be commensurate ..." This makes it clear that a summary is permissive not required. Further, applicants point out that the Examiner's objection is contrary to the practice of the USPTO, which routinely issues patents that do not have summaries. The applicants have amended the specification to include the now known serial number and filing date of the related application.

The Examiner's objection to the drawings and the rejection for lack of enablement was on the same grounds so the applicants' response will address them together. The Examiner pointed to the "enable signal" and "timing signal" as lacking. In this regard, point out that the claimed enable signal is supported by the output of column decoder 22 which is present in FIGs. 2-4 and described at page 7, lines 8 and 9. Similarly, the claimed timing signal is supported by the output of timing circuit 20 in FIGs. 2-4 and described at page 7, lines 9 and 10. The Examiner asked about how the claimed switch circuit is responsive to these signals. The switch circuit as claimed is supported by NAND gate 108 and transistor 110 as shown in FIGs. 2-4. That these signals cause transistor 110 to be conductive is described at page 7, lines 8-15.

The Examiner questioned the support for second switch circuit coupled between the second terminal of the switch circuit and the voltage reference as recited in claim 10. The second switch is supported by transmission gate 116 shown in FIG. 3 and is connected as described in the claim. This is described in the specification at page 9, lines 10-13.

The Examiner questioned the support for feature recited in claim 13. Claim 13 has been amended by adding the phrase "further comprising" which is the more common phrasing for this type of dependent claim. The claimed second switch is supported by transmission gate 116 of FIG. 3 and described at page 9, lines 10-13.

The Examiner questioned the support for group of memory cells of the plurality of memory cells as recited in claim 14. Each group of memory cells is supported by the memory cells coupled to a particular write line. This is shown in FIG. 1. For example, one such group of memory cells 60, 68, 76, and 84 are coupled to write line 52. Exemplary writing of a single cell of the group is described at page 4, line 22, to page 5, line 15.

The Examiner questioned the support for a second plurality of transistors, a second plurality of switch circuits, and the second enable signal and timing signal. This is supported by FIG. 1 in combination with any of FIGs. 2-4. FIG. 1 shows a plurality of write drivers for the row write lines. Each of the write drivers is the same as write driver 36 in construction but receives row signals instead of column signals. Similarly row bias circuit 26 is the same as column bias circuit in construction but is connected to row drivers. This is pointed out at page 14, lines 7-13. Thus, the support for the claimed second plurality of transistors is transistor 14 that is present in row drivers 28-34. Similarly, the claimed second plurality of switch circuits is supported by NAND gate 108 and transistor 110 that are present in row write drivers 28-34.

The Examiner questioned claim 19. Claim 19 has been cancelled.

The Examiner questioned the support in claim 20 for the plurality of the second switch circuits. This is supported by transmission gate 116 as is present in write drivers 36-42.

The Examiner questioned the support for the feature of claim 22. The current mirror operation is described at page 7, lines 17-21. The current mirror is between transistors 104 and 114 as shown in FIGs. 2-4.

The Examiner questioned claim 27. Claim 27 has been cancelled.

The Examiner pointed out a lack of antecedent basis for "switch circuit in claims 1, 2, and 10. Claims 1, 2, and 10 have been amended. The Examiner also pointed out lack of antecedent basis in claims 14, 15, 17, 31, and 32. These have also been corrected by amendment except for the line 14 objection to claim 14. The earlier change to claim 14 established that there was a current. Although lacking antecedent basis, applicants submit that none of these claims lacked clarity as to what was being claimed.

The rejection for obviousness was based on Ito. In this regard, the only operation that is described in detail is a read operation. The write operation is described only generally by stating that a current is passed through the write word lines and the bit lines. There is no description as to what circuits are used to provide these currents. Ito has another patent, US Patent No.

6,693,822, see the description of FIG. 3 in particular, in which the write circuit is described, and it is quite different from the read circuit of the reference cited by the Examiner.

As for the dependent claims, even the circuit that supplies the current on the bit lines as described for a read operation is deficient. For example, claim 10 requires a capacitor. Applicants have not been able to find any capacitor in the current driver circuit of Ito, much less one that meets the requirements of the claim. Similarly for the second switch of claim 13 and other claims, applicants have not been able to find an analogous element in Ito.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Applicants believe the application is in condition for allowance which action is respectfully solicited. Please contact the below-signed if there are any issues regarding this communication or otherwise concerning the current application.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079.

Respectfully submitted,

SEND CORRESPONDENCE TO:

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